ThalesAlenia Space
A Thales / Finmeccanica Company

Next generation of telecom payload and impact on PCB

PCB workshop, Noordwijk – October 22nd & 23rd, 2009

THALES

Outline

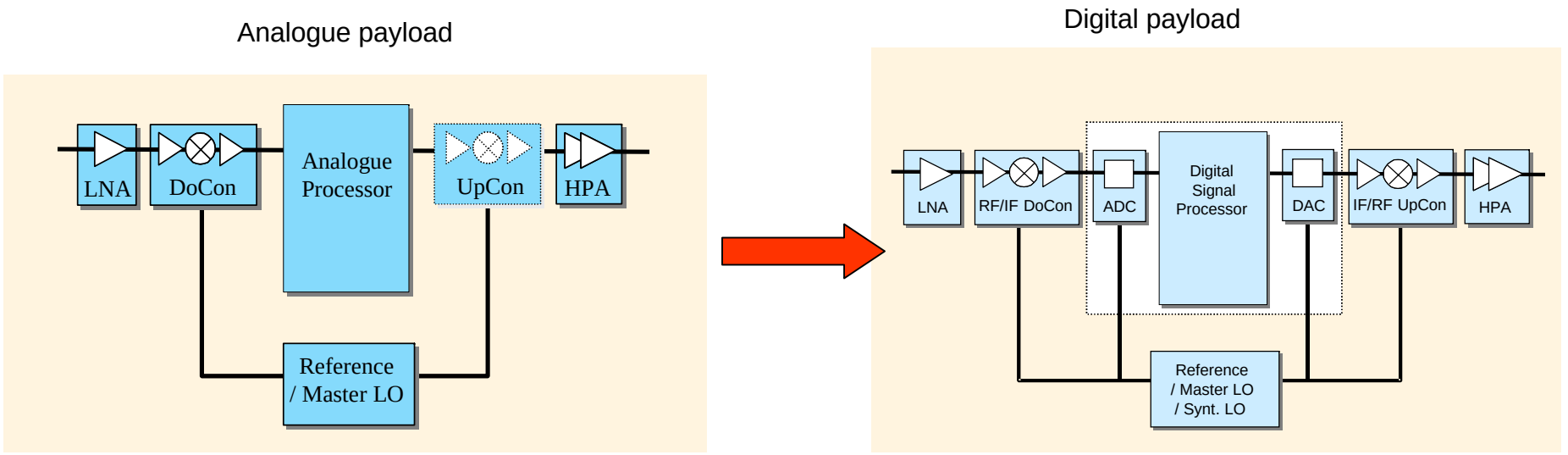
- Telecom payload requirement
- Impact on PCB
- PCB requirement : TAS vision
- Conclusion

Telecom payload requirement

- Increasing capacity payloads due to depleting orbital resources with higher number of beams and larger aggregate bandwidth
- New market based on broadband communications: high data rate connections to very large numbers of low-cost terminals
- Meeting the evolution of the needs over the average 15 years of a satellite lifetime
- New satellite payloads have to meet such requirements of larger bandwidth, system transparency and flexibility

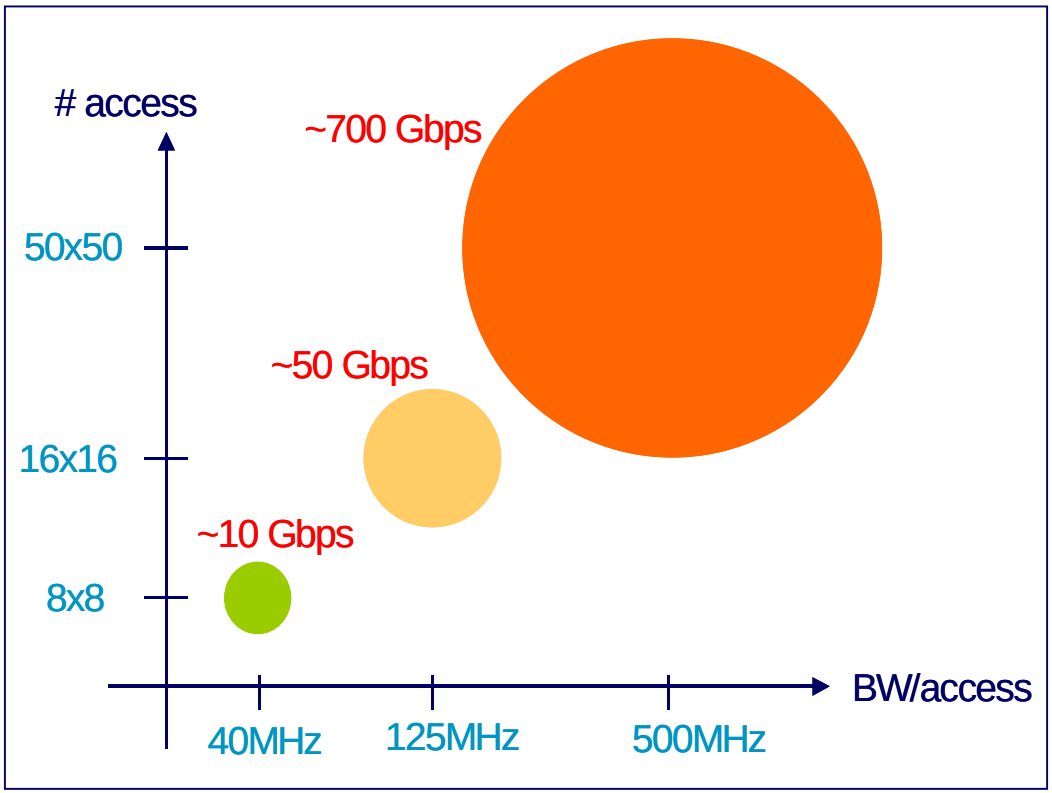
Telecom payload requirement

- Digital transparent processor is a nice example to such advanced telecom repeater subsystems
  - Analogue to digital (ADC) and digital to analogue (DAC) converters
  - Digital processing enabling flexible beam to beam connectivity for example



Telecom payload requirement

- Digital transparent processors demand for high throughput
  - above 1 Tbps range for DTP (for example 10 Tbps if 200 accesses with up to 1 Ghz bandwidth per access are considered)



Telecom payload requirement

- Digital transparent processors face design constraints
  - Surface & volume
  - power consumption
- Integration mandatory
  1. High pin count packages
     - «BGA» packages with 1600 I/Os
     - Dimensions of 42,5 mm x 42,5 mm
     - Pitch of 1mm
     - Power : 10 to 15 watts
  2. High data rate links (6.25 Gbps) and high numbers of links (up to 200?)
  3. High frequency analogue signals get along with high data rate digital signals

Impact on PCB

- Base material
  - Coefficient of Thermal Expansion (CTE) suitable for a reliable mounting
  - High glass temperature
  - Good thermal performances
  - Good electrical performances : dielectric constant and low loss figures
  - Compatible with new regulations (RoHs, Reach, environment)

- Design rules
  - Compatible with the need to route 800 functional I/Os per ASIC
  - High density interconnect PCBs
  - High number of layers with different controlled impedance per layer
  - Close to the best-in-class available for harsh environment (cost, lead-time,…)

PCB requirement : TAS vision

- µvia technologies are required
- Copper filled µvia in pad to allow denser design
- Embedded passive components for high speed design
- PCB structure embedding RF layers for high frequency analogue signals
- Conductor width / spacing enabling routing of differential signals between two adjacent vias distant of 1 mm
- Optical links to interconnect boards : optical flex, optical waveguides in PCB,…

Conclusion

- The PCB has to be considered as an active interconnect component
- To succeed in our projects, we need
  - PCB technologies at the right level of technicality for each project
  - Close to market standard (standardization, cost, lead-time)
  - Qualified industrial sources by Space Agencies

Thank for you attention